Notice of Allowability	**Application No.** 10/681,856	**Applicant(s)** CHAI ET AL.
	Examiner Mujtaba K. Chaudry	**Art Unit** 2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *11/28/2005*.

2. ☒ The allowed claim(s) is/are *1,7,12-14 and 20*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 7/19/2005
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *1/20/2006* .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

GUY LAMARRE
PRIMARY EXAMINER

1/20/06

EXAMINER'S AMENDMENT

An Examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to Applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this Examiner's amendment was given in a telephone interview with Jack P. Friedman (518-220-1850) on Friday, January 20, 2006.

The following claims are the only remaining claims in the present application.

Please amend the claims in the application as follows:

Please replace Claim 1 with:

1. A plurality of memory arrays, each memory array comprising:

a compilable address magnitude comparator, the compilable address magnitude comparator of each memory array receiving a self-test address from a self-test controller and comparing the self-test address to a compiled maximum address of each memory array, the compilable address magnitude comparator of each memory array preventing testing of memory of each memory array corresponding to the self-test address if the self-test address exceeds the compiled maximum address of each memory array;

wherein the compilable address magnitude comparator of each memory array prevents testing of memory of each memory array by forcing a memory pass signal;

wherein the compilable address magnitude comparator of each memory array includes a row comparator and a column comparator, the row comparator comparing a self-test row address of each memory array and the column comparator comparing a self-test column address of each memory array; and

wherein the compiled maximum address of each memory array comprises a maximum row address of each memory array and a maximum column address of each memory array;

wherein the compilable address magnitude comparator of each memory array prevents testing of memory of each memory array by forcing a read operation instead of a write operation.

Please cancel Claim 4:

4. (Cancelled)

Please replace Claim 7 with:

7. A plurality of memory arrays, each memory array comprising a compilable address magnitude comparator, the compilable address magnitude comparator of a memory array of the plurality of memory arrays comprising:

a row comparator, the row comparator comparing a row portion of a self-test address from a self-test controller with a compiled maximum row address, the compiled maximum row address corresponding to a maximum valid row address of the memory array; and a column comparator, the column comparator comparing a column portion of the self-test address with a compiled maximum column address of the memory array, the compiled maximum column address corresponding to a maximum valid column address of the memory array;

wherein the compilable address magnitude comparator modifies a self-test operation of the memory array when either the row portion of the self-test address exceeds the corresponding maximum valid row address of the memory array or the column portion of the self-test address exceeds the corresponding maximum valid column address of the memory array;

wherein the compilable address magnitude comparator prevents testing of memory of the memory array by forcing a memory pass signal in a corresponding built-in-self-test controller;

wherein the compilable address magnitude comparator prevents testing of memory of the memory array by forcing a read operation instead of a write operation; and

wherein the row comparator includes at least one logic block selected from a plurality of logic blocks, with each of the plurality of logic blocks corresponding to a portion of a compiled maximum address of the memory array such that by selecting one of the plurality of logic blocks, the compilable magnitude comparator tests for the compiled maximum address of the memory array.

Please replace Claim 12 with:

12. An application specific integrated circuit, the application specific integrated circuit comprising:

a plurality of memory arrays, each memory array comprising a compilable address magnitude comparator;

a built-in-self-test controller coupled to each memory array, the built-in-self-test controller testing the memory of each memory array;

wherein the compilable address magnitude comparator in each memory array receiving a self-test address from the built-in-self-test controller and comparing the received self-test address with a compiled maximum address of each memory array;

wherein the compiled maximum address of each memory array corresponds to the highest valid address for each memory array;

wherein the compilable address magnitude comparator of each memory array prevents the built-in-self-test controller from testing a memory location of each memory array corresponding to the self-test address if the self-test address exceeds the compiled maximum address of each memory array;

wherein the compilable address magnitude comparator of each memory array prevents testing of memory of each memory array by forcing a read operation instead of a write operation; and

wherein the compilable address magnitude comparator of each memory array prevents testing of memory of each memory array by further forcing a memory pass signal, and wherein a second memory array of the plurality of memory arrays has a different maximum number of columns than does a first memory array of the plurality of memory arrays.

Please replace Claim 13 with:

13. The application specific integrated circuit of claim 12, wherein the compilable address magnitude comparator of each memory array includes a row comparator and a column comparator;

wherein the row comparator of each memory array compares a self-test row address and the column comparator of each memory array compares a self-test column address.

Please replace Claim 14 with:

14. The application specific integrated circuit of claim 12, wherein the compiled maximum address of each memory array comprises a maximum row address of each memory array and a maximum column address of each memory array.

Please replace Claim 20 with:

20. The application specific integrated circuit of claim 12, wherein the comparator of each memory array is compilable by selectively substituting a plurality of compilable logic blocks according to the compiled maximum address of each memory array.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

Mujtaba Chaudry
Art Unit 2133
January 20, 2006

GUY LAMARRE
PRIMARY EXAMINER